

SOLEIL HW/SW DAQ experience and future plan

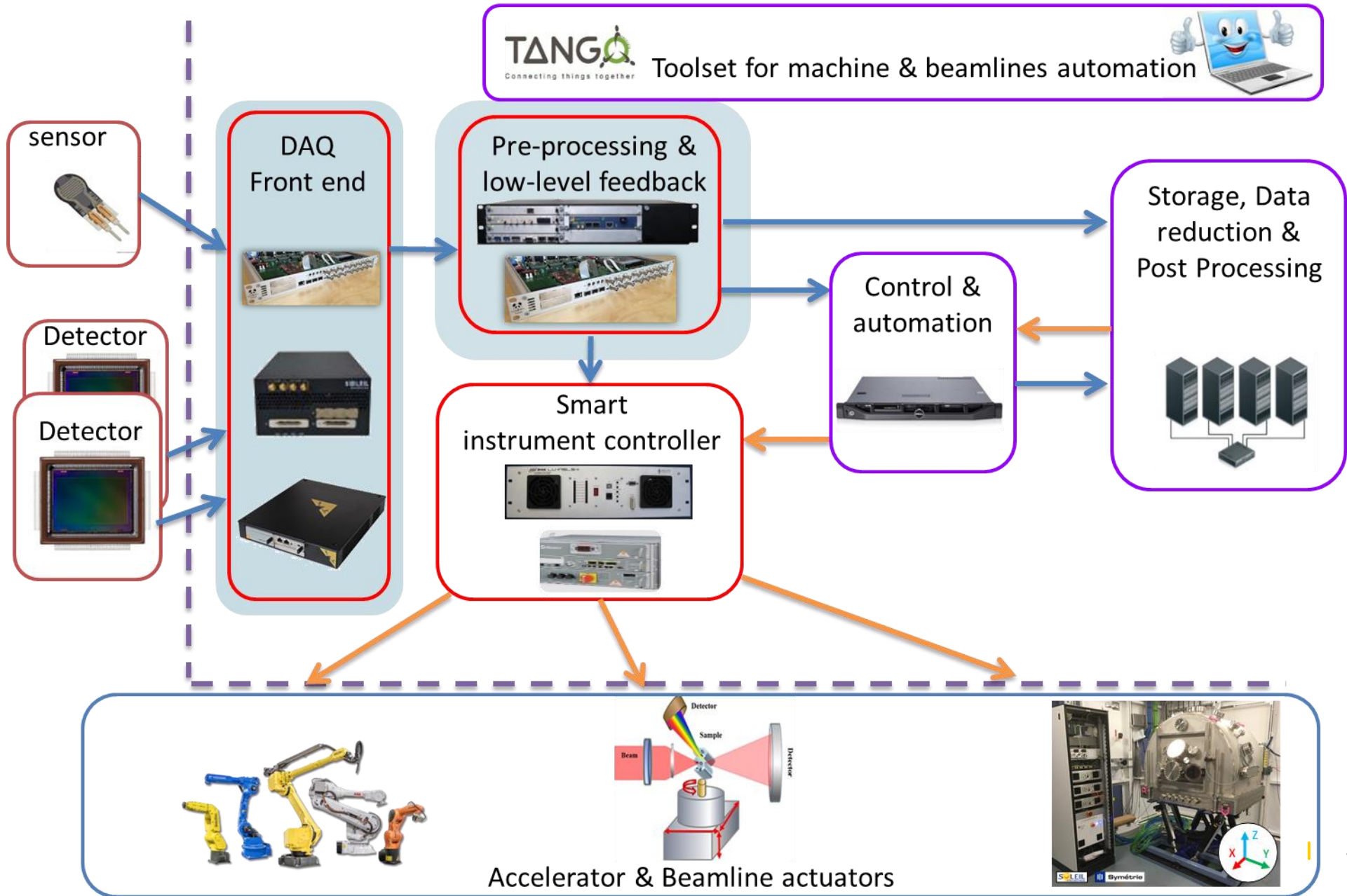
Yves-Marie ABIVEN – Florent LANGLOIS

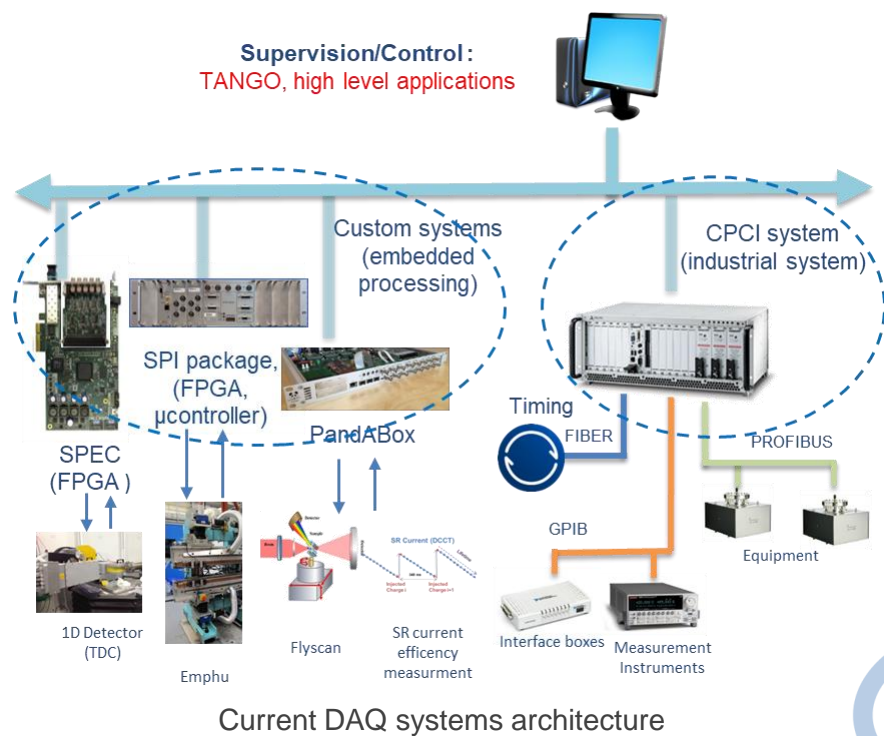
- Hardware acquisition systems
 - MACUP project
 - PandABox and MicroTCA studies and developments
- Software acquisition systems
 - Scans
 - ScanServer
 - Flyscan
 - Detectors
 - Lima
 - MCAs
- Perspectives



SOLEIL hardware acquisition systems







Current DAQ systems architecture

Currently on production:

- 271 CPCI CPUs (~200 crates)
- ~1000 CPCI IO cards
- ~50 ETH standalone products (including 35 PandABox)
- 113 SPI cards

See control presentation,
P.Rommelueère

Analysis, Synthesis of
architecture proposals,
Operational solutions

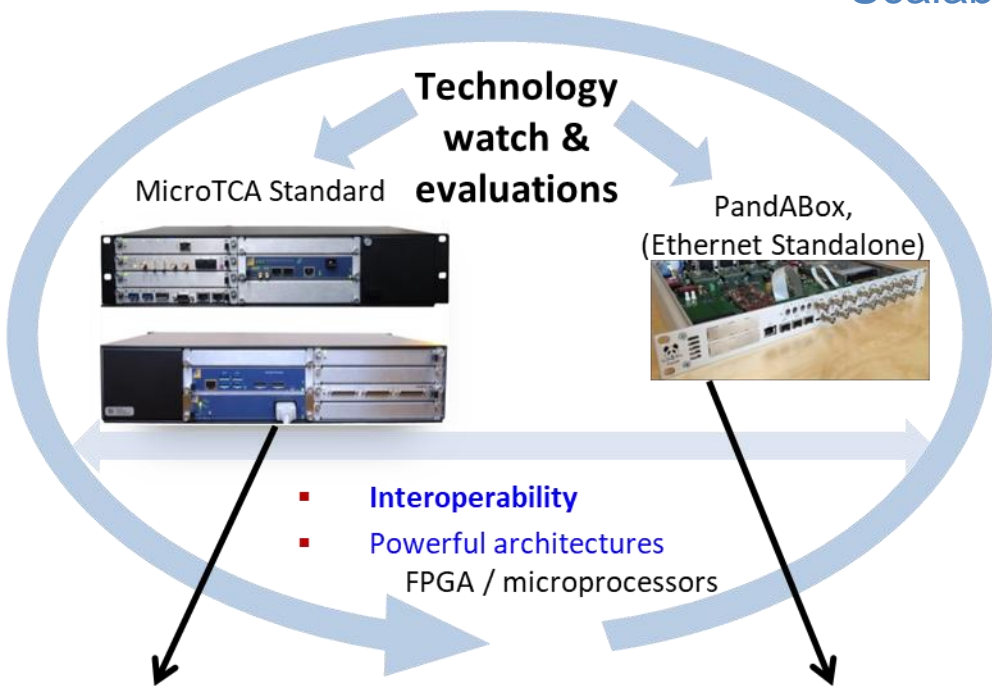
■ Motivations

- Maintain installed acquisition systems at their **best performance level** (MOC: Maintains in Operational Conditions) and **anticipate the obsolescence** of the acquisition systems (e.g., sustain the systems)
- Improve the acquisition systems by delivering higher **performance** and better **embedded processing capacity**, and **answer new emerging needs**

■ Selected strategies

- Deal with **obsolescence** of the acquisition systems
 - Industrial computer. Homogenize CPU/OS (3 CPUs/3 OS -> 1 CPU/1 OS)
 - Lighten the catalog of functions managed by the CPCI → PLC, Ethernet standalone products ...
 - Migration obsolete **FPGA based products** to successors like **PandABox**
- Offer **new architectures**, hardware and software **solutions** to meet emerging requirements (**standardize "generic" platforms, firmware and embedded software**)

Scalable FPGA/SoC technology

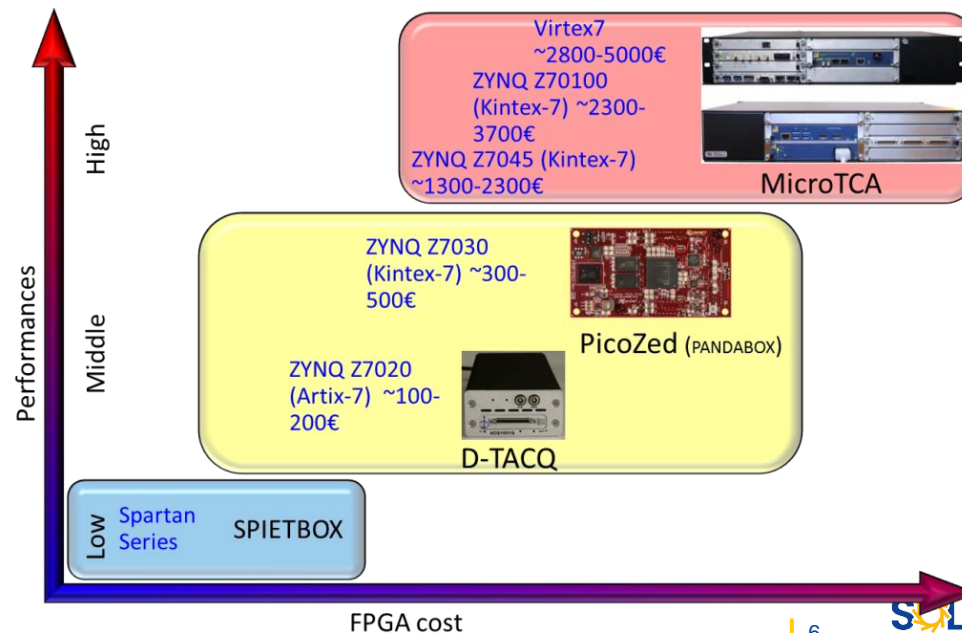
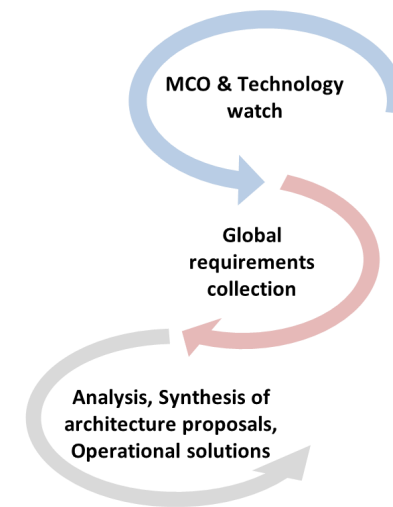


Well adapted for **demanding applications** such as LLRF, Position feedback from 2D detector, development of large detector. Technology intended for medium – long term

Under development

Well dimensioned for short term requirements such as improving scanning application, developing small detectors.

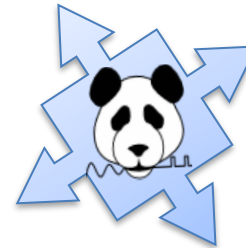
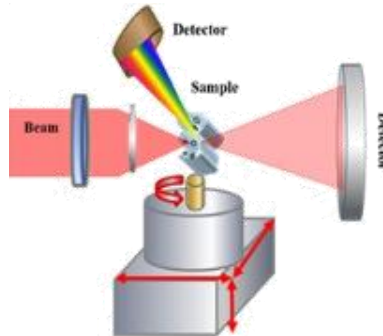
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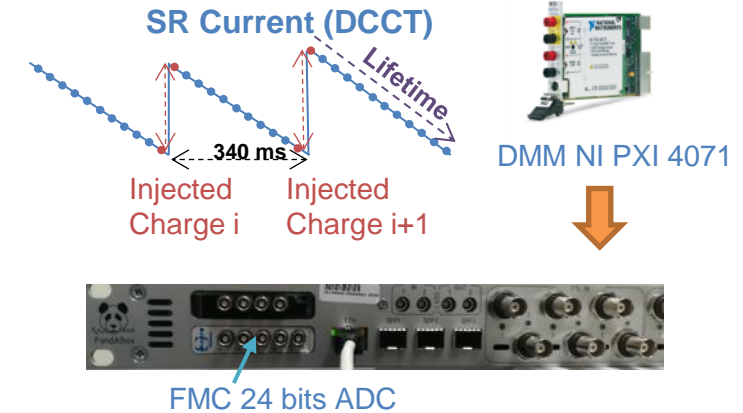
- UFX detector DAQ interface



- Continuous scan applications (Flyscan)

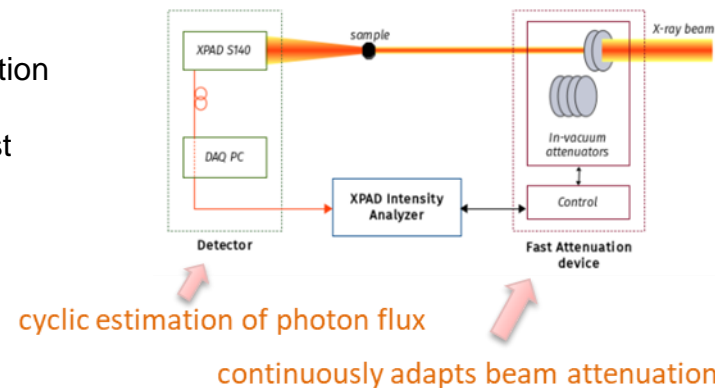


- CIEL (Current Injection Efficiency and Lifetime) :
 - New acquisition system for the DCCT



- FastATT XPAD: Upgrade of the real-time control system for the Fast beam-ATTenuation with an XPAD detector

Global architecture of the XPAD controlled beam-attenuation system



- Beamline DAQ systems upgrade:
 - QEXAFS monochromator position and ionization chamber captures → [On going project](#)
 - Strain gauge measurement for the fatigue test machine
 - Nanoprobe interferometers position captures
 - ...

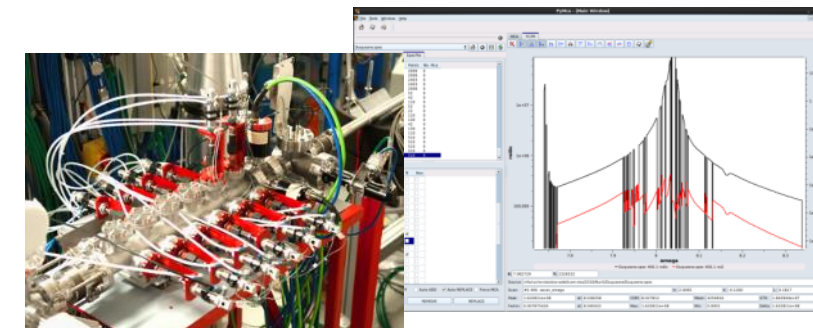


Fig.: attenuation system installed on the SixS beamline at SOLEIL

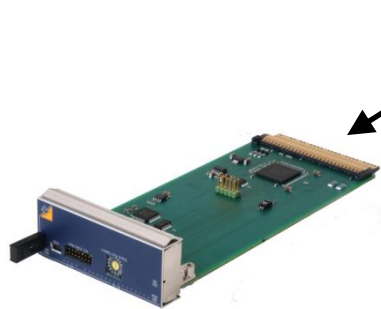
NATIVE-R2
6 AMCs, 5 μ RTMs, PM, JSM, MCH, MCH-RTM

- 2U MTCA.4 chassis for AMCs and μ RTMs and JTAG Switch Module



NAT-MCH-PHYS80 MTCA Carrier Hub for MTCA.4 and MTCA.4.1 applications supports GbE and PCIe Gen 3 switching and optical & copper PCIe x8/x16 uplinks

NAT NATIVE-mini
Smallest (1U) MicroTCA-chassis for industrial applications, with integrated MCH

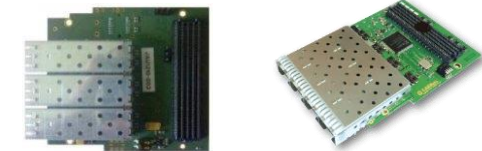


NAT-JSM
JTAG Switch Module



AMC for DAQ & signal processing applications and computing nodes based

- NAT NAMC-ZYNQ-FMC: FMC Carrier AMC with Xilinx Zynq-7000 FPGA SoC (EOL)
- NAT NAMC-ZYNQUP -FMC: FMC Carrier AMC with Xilinx Zynq UltraScales+ FPGA MPSoC
- CAENels DAMC-FMC2ZUP: FMC HPC& FMC+ Carrier AMC with Xilinx Zynq UltraScale+ MPSoc



FMC SFP+ & 4SFP+
High throughput Interface

+

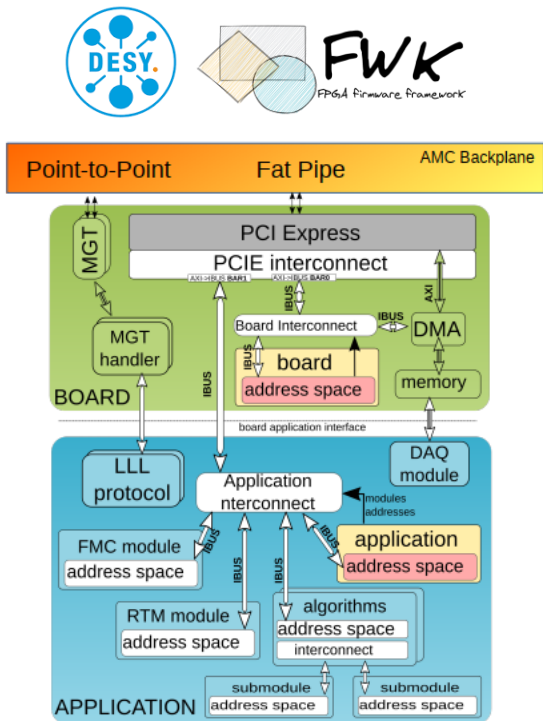


FMC Firefly module (14Gbps x 10)



FMC ADC/DAC/DIO modules

Modular Interfacing & Processing

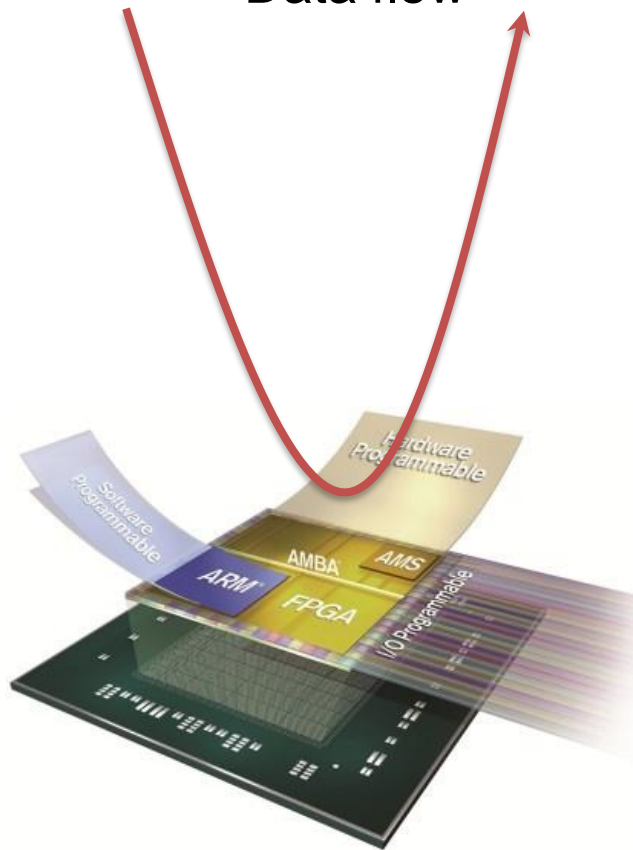


Gateway*

* Schema not up to date

Modular

Data flow



Powerful

Control Framework Ready

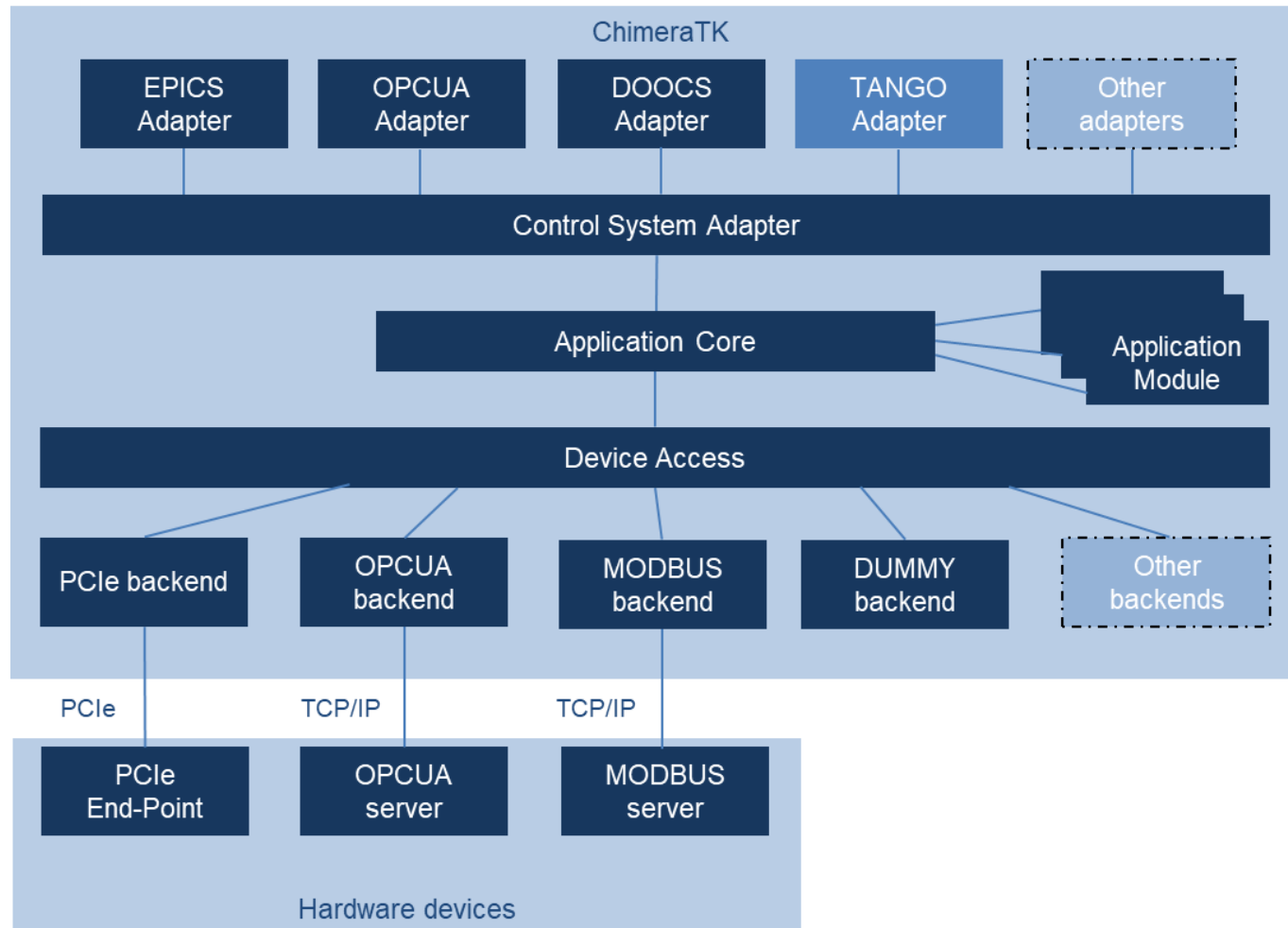


Software

Connectable

Flexible Framework architecture
for embedded processing and connectivity for Control and DAQ

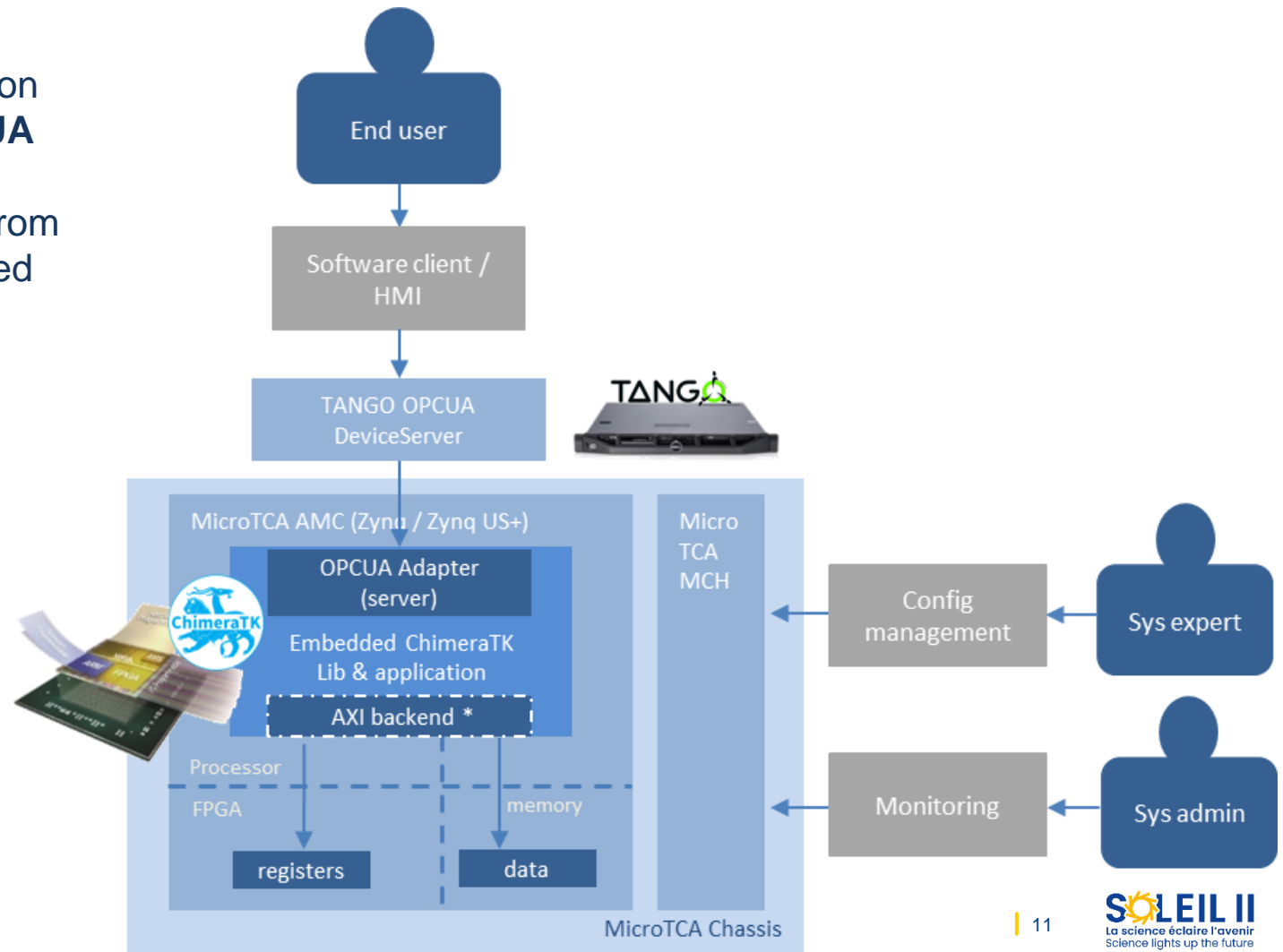
- Control system and Hardware Interface with Mapped and Extensible Register-based device Abstraction Tool Kit
- Developed by DESY
- ChimeraTK “Tango Adapter” is under development at SOLEIL



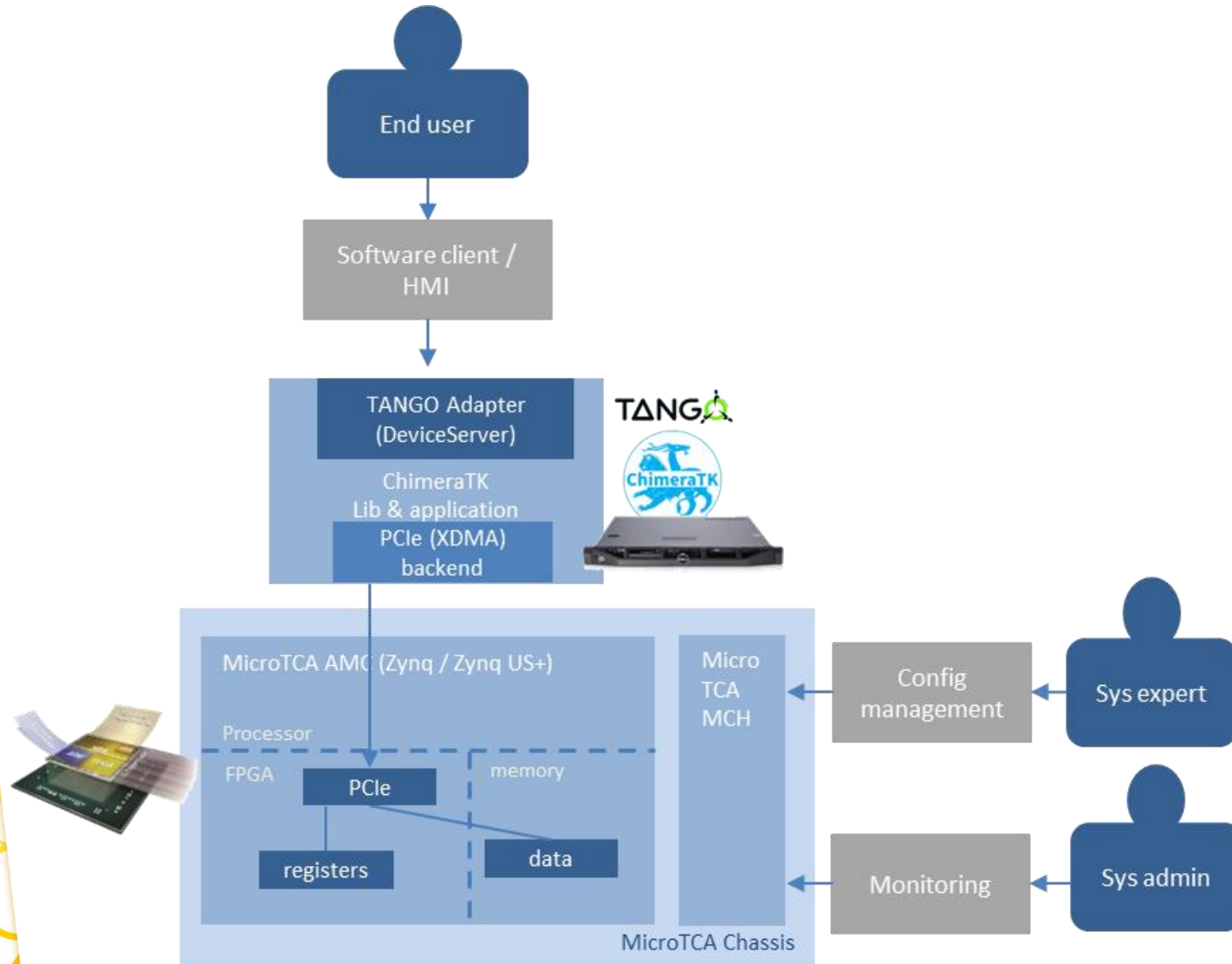
2 selected complementary architectures:

Solution 1: remote TANGO DeviceServer communicates with **ChimeraTK embedded** on the MTCA Zynq PS over Ethernet and **OPCUA** protocol

- Embedded ChimeraTK takes FPGA data from AXI bus to the custom process implemented on its Application level, and expose processed data to the OPCUA Adapter (server)
- * ChimeraTK “AXI (UIO) backend” development just released by DESY



2 selected complementary architectures:



Solution 2: ChimeraTK with “TANGO Adapter (DeviceServer)” on the control server, communicates with MTCA FPGA over **PCIe-over-fiber** link

- ChimeraTK takes FPGA data from PCIe link to the custom process implemented on its Application level, and expose processed data to the TANGO Adapter (DeviceServer)
- PCIe-over-fiber’s hot-swapping feature needs to be studied → **Evaluated but not stable**

- Applications

- [FOFB upgrade](#) (Diags group collab)
- DLLRF upgrade (RF group)
- Fast acquisition: e.g. ADC for QuickExafs, digitizer for filling pattern measurement etc.

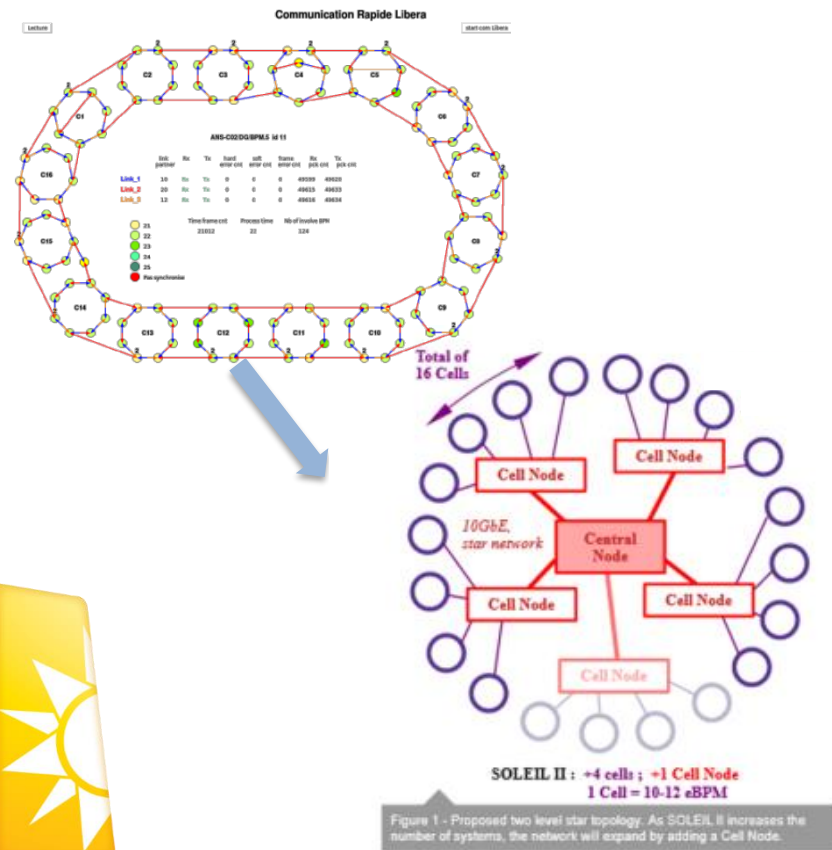
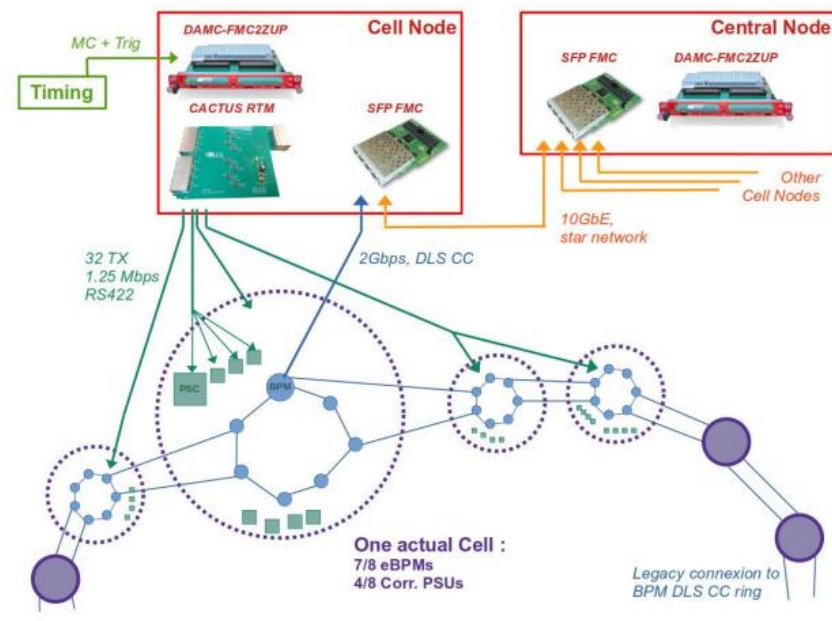
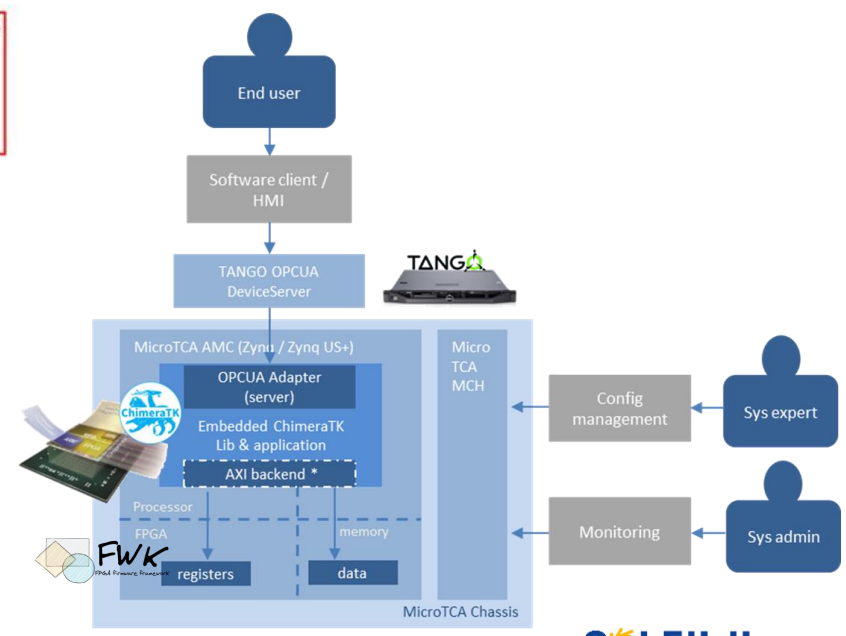


Figure Proposed two level star topology. As SOLEIL II increases the number of systems, the network will expand by adding a Cell Node.



System integration. One Cell node is connected to 4 cells.



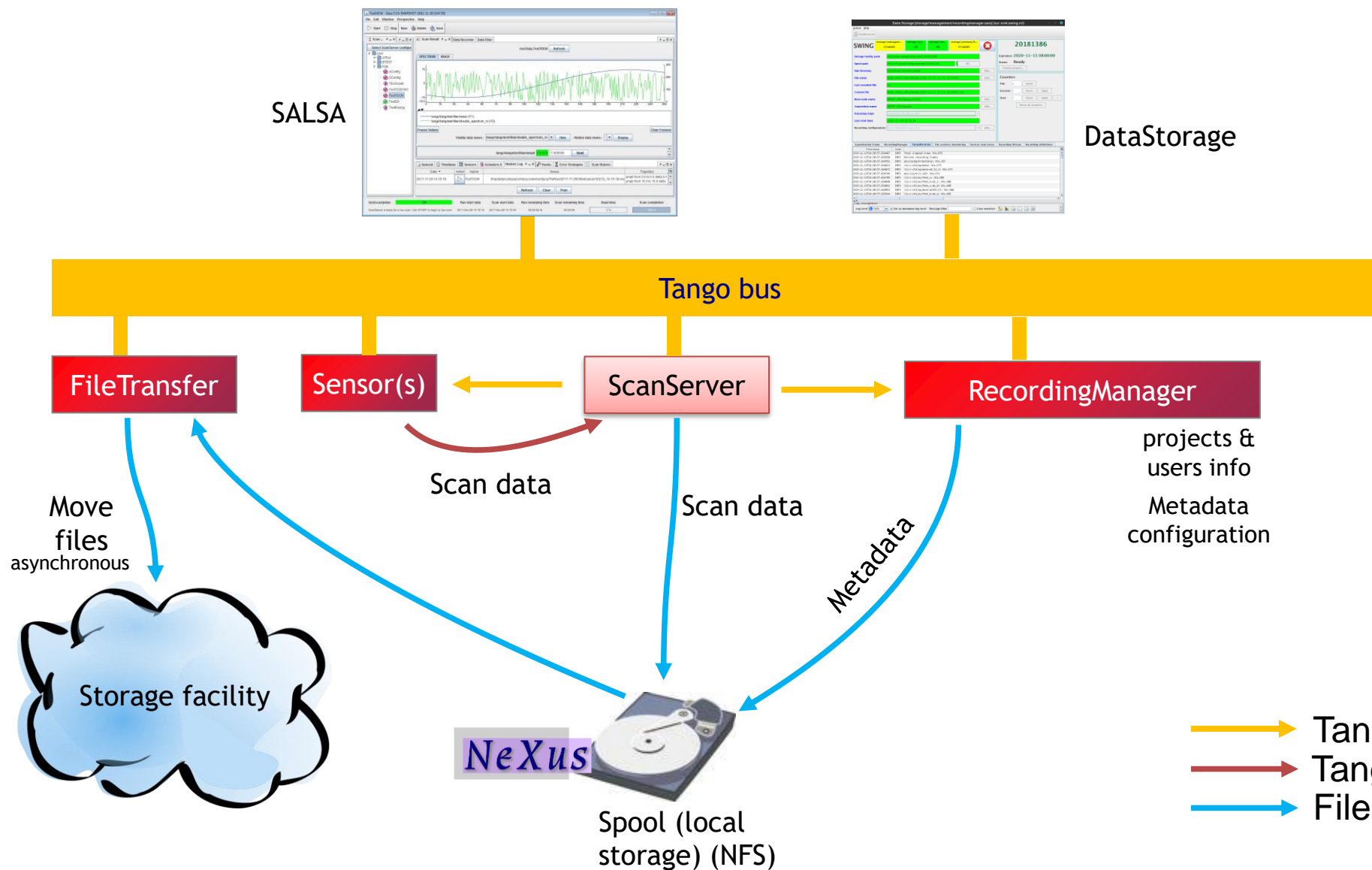
SOLEIL software acquisition systems



- Generic Tango DeviceServer (C++)
- 1D / 2D step scans
- Plugins system (68)
- Easily configurable by users
- ISAC Clients integration
- Legacy system
- Does the job since 2005 on ~85 % of Beamlines !!!

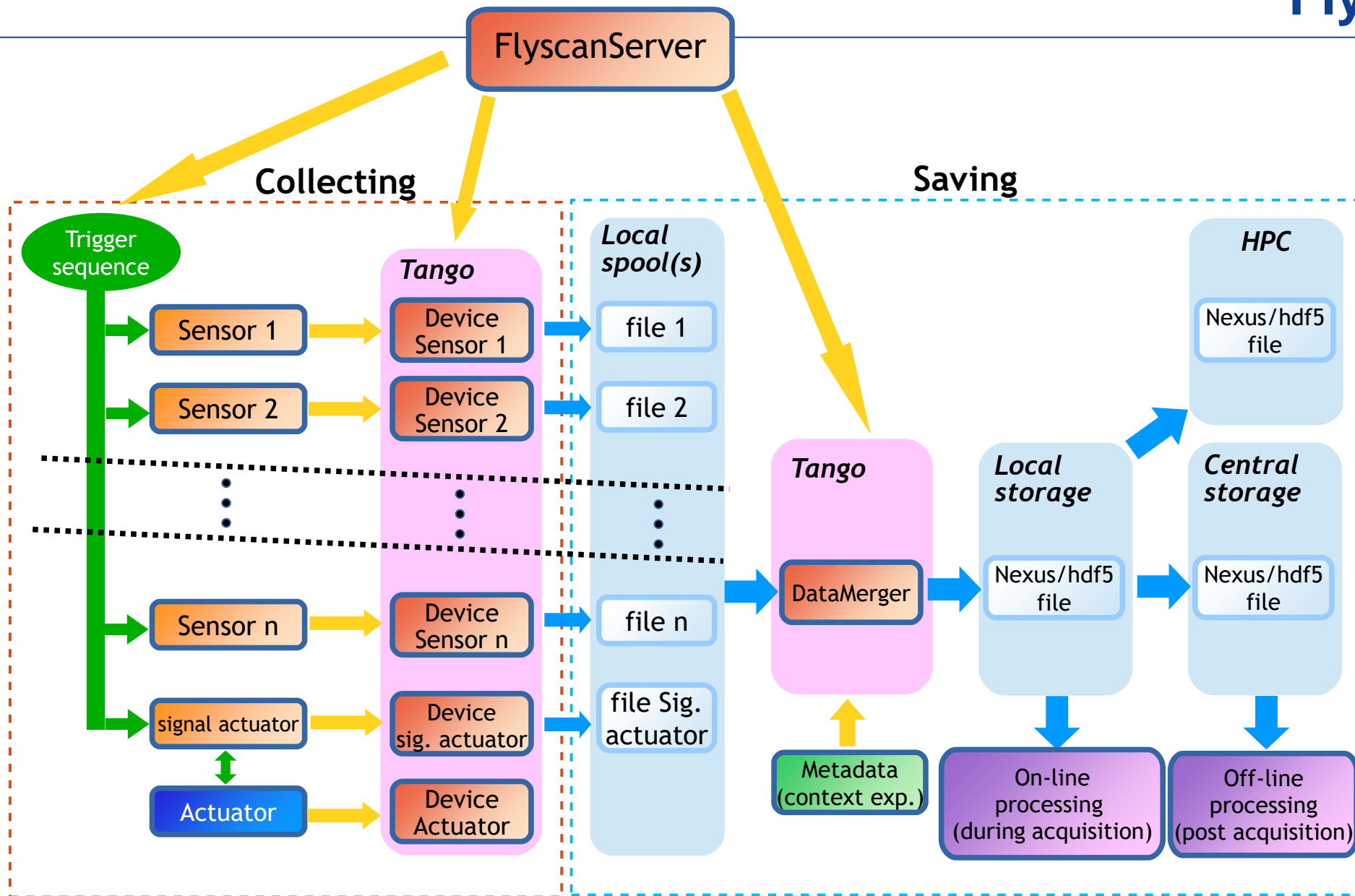
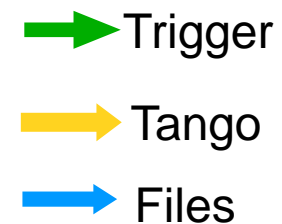
The screenshot displays the ScanServer interface for a scan named "root.spjz.Test1D1Actuator1Sensor". The main window shows a "SPECTRUM" plot with a red curve representing the scan data. Below the plot, there are "Freeze Values" for two parameters: "tango/tangotest/spjz_01.01/short_scalar_w" with a value of 1940, and "tango/tangotest/spjz_01.02/double_scalar" with a value of 308.19. The interface includes a "Scan Manager" tree on the left, a "Display Manager" on the right, and a "General" tab at the bottom. The status bar at the bottom indicates the scan is "MOVING" and "RUNNING" with a completion of 97.00%.

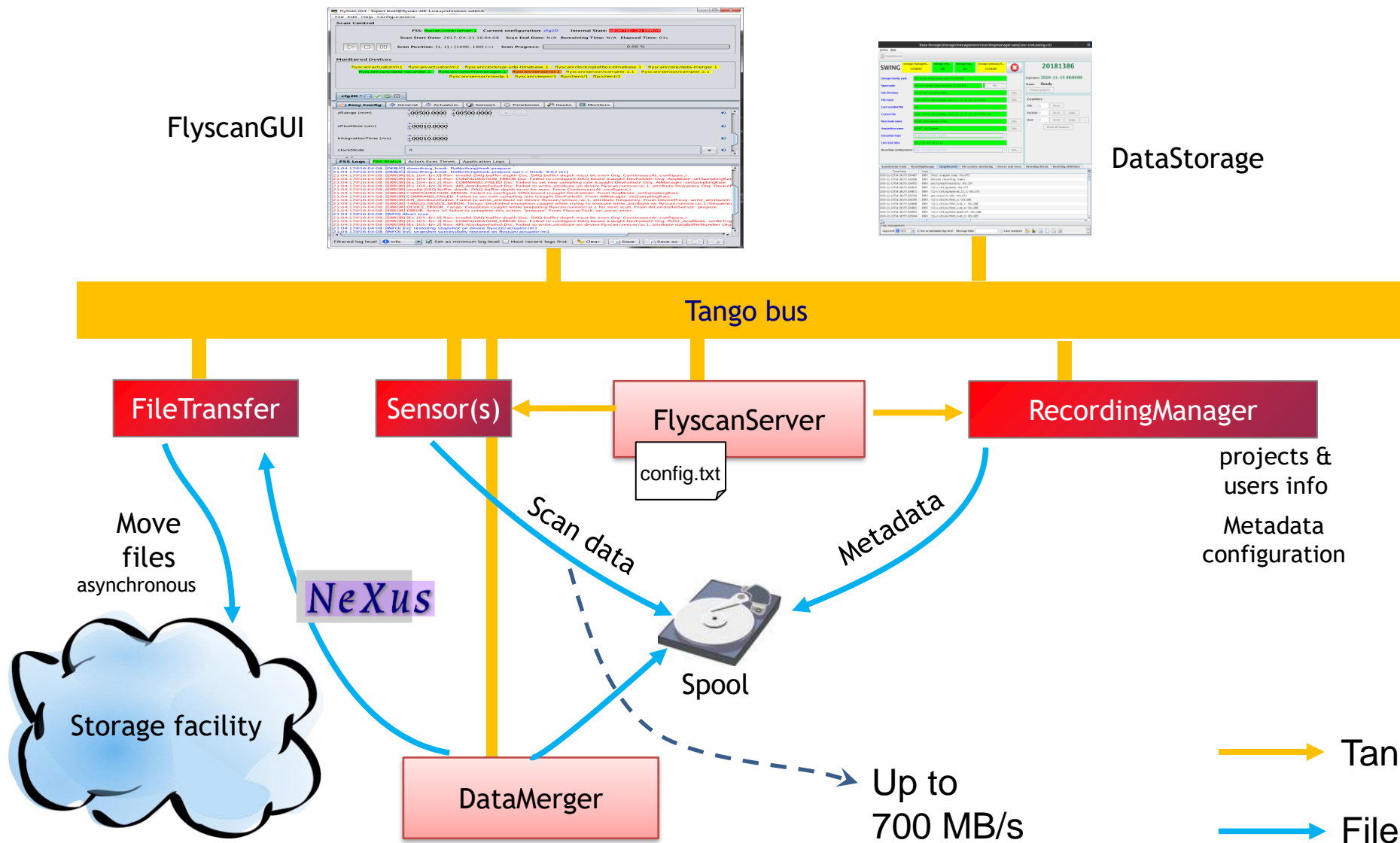
ICA/SALSA/SCAN.1	MOVING	Run start date	Scan start date	Run remaining time	Scan remaining time	Dead time	Scan completion	Scan number	X Point
Scan in progress		16:02:58	16:02:58	00:00:03	00:00:03	1.000 %	97.00 %	01	98/101



- Tango DeviceServer (C++)
 - With plugins (52 in C++ / python)
 - Continuous and step scans in N dimensions
-
- Project started in 2010
 - In production since 2014
 - On 14 BL (out of 29)
 - Number of configs: ~ 30 (one config = one acquisition, e.g. mesh, Tomo ...)
 - Complex configs : by ctrl people







FlyScan GUI - Expert level@flyscan-el6-1.lica.synchrotron-soleil.fr

File Edit Help Configurations

Scan Control

FSS: flyscan/core/server.1 Current configuration: cfg2D Internal State: **ABORTED ON ERROR**

Scan Fly Scan Visu 3.5.16-8028

File Edit Images Help

Cartography

Transformation: None

Ca

Zoom: 265% axes: [out] Show Statistics

Cu

Zoom: 265% axes: [out] Show Statistics

Pb

Zoom: 265% axes: [out] Show Statistics

Mn

Zoom: 265% axes: [out] Show Statistics

Fe

Zoom: 265% axes: [out] Show Statistics

Zn

Zoom: 265% axes: [out] Show Statistics

Monitored Devices

- flyscan/actuator/m1 fly
- flyscan/core/data-rec...

cfg2D *

Easy Config **General**

zRange (mm) -0.77

zPixelSize (um) +0.77

integrationTime (ms) +0.77

clockMode 0

FSS Logs **FSS Status** **Ac**

```

21.04.17@16:04:08: [DEBUG] dor
21.04.17@16:04:08: [DEBUG] dor
21.04.17@16:04:08: [ERROR] [Ex
21.04.17@16:04:08: [ERROR] [Ex
21.04.17@16:04:08: [ERROR] [Ex
21.04.17@16:04:08: [ERROR] [Ex
21.04.17@16:04:08: [ERROR] inv
21.04.17@16:04:08: [ERROR] CO
21.04.17@16:04:08: [ERROR] CO
21.04.17@16:04:08: [ERROR] AP
21.04.17@16:04:08: [ERROR] TA
21.04.17@16:04:08: [ERROR] DE
21.04.17@16:04:08: [ERROR] ERR
21.04.17@16:04:08: [INFO] Abor
21.04.17@16:04:08: [ERROR] [Ex
21.04.17@16:04:08: [ERROR] [Ex
21.04.17@16:04:08: [ERROR] [Ex
21.04.17@16:04:08: [ERROR] [Ex
21.04.17@16:04:08: [INFO] [rz]
21.04.17@16:04:08: [INFO] [rz]

```

Filtered log level **info**

flyscan/core/viewer.1

data-merger has switched to state STANDBY

Motor positions

106-M-CX/EX/GONIO.2-MT_Ts.2	-1.1786	Send	-1.9940 mm	STANDBY
106-M-CX/EX/GONIO.2-MT_Tz	-11.3566	Send	-11.2635 mm	STANDBY

- **Python interface & ipython profile**

```
In [9]: fss.cfgs.cfg2D.easy_config.parameters
Out[9]:
EasyConfigProp()
+- clockMode ..... 0
+- integrationTime ... 10.0
+- split ..... 1
+- xPixelSize ..... 100.0
+- xRange ..... [-10000.0, 10000.0]
+- xrf_config ..... {"P": [400, 430], "K": [652, 689], "S": [452, 485], "Cl": [516, 552]}
+- zPixelSize ..... 200.0
+- zRange ..... [-500.0, 500.0]
```

- **SPYC (SOLEIL's Python Command line interface) integration**
- **FlyscanViewer Tango device**
 - Display data during acquisition as Tango attributes from final Nexus file
 - Plugin system to do some data reduction



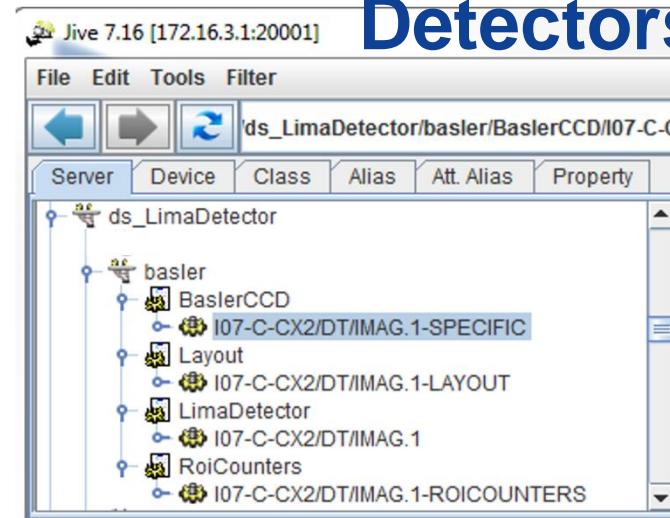
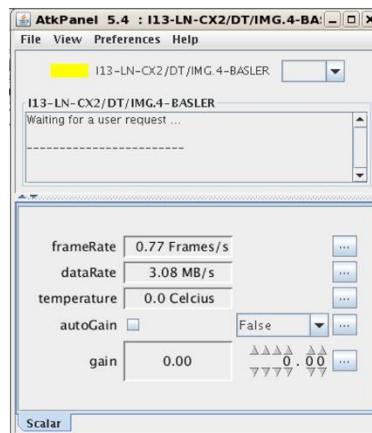
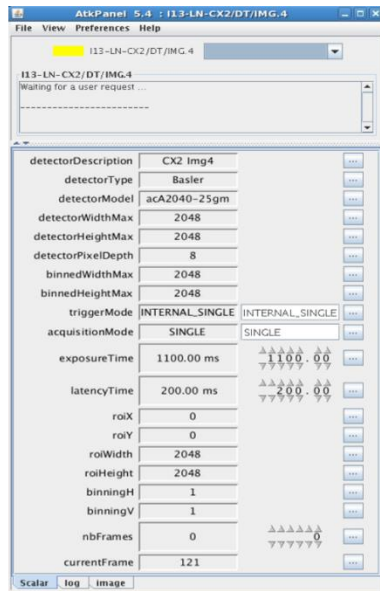
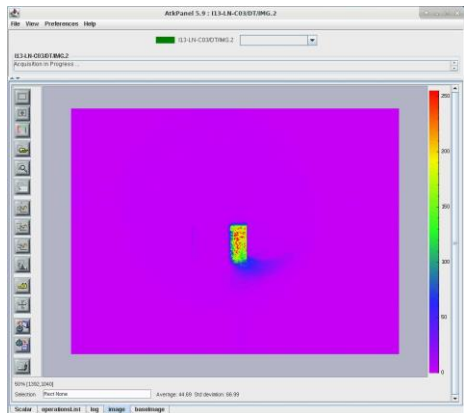
- Library for **IMage Acquisition**
- C++ with Python interface
- **Generic** part with standard interface
- **Plugin** system to handle camera **specific** stuff
- Collaboration with ESRF, ALBA, MAX4, DESY
- **21** Camera type supported at SOLEIL (45 in total)
- Basler (Beam Monitoring), Hamamatsu, Eiger, Pco ...
- **301** instances (200 Basler)

#	Detector	NB instance	#	Detector	NB instance
1	Andor	1	15	RoperScientific	3
2	Basler	200	16	SLSEiger	1
3	Dhyana	8	17	SLSJungFrau	1
4	Eiger	3	18	SpectralInstrument	1
5	Hamamatsu	15	19	SpectrumOne	1
6	ImXpad	8	20	UFXC	2
7	Lambda	3	21	Uview	1
8	Marccd	1			
9	Maxipix	1			
10	Merlin	10			
11	Pco	9			
12	PerkinElmer	1			
13	Pilatus	4			
14	Princeton (Teledyne)	1			

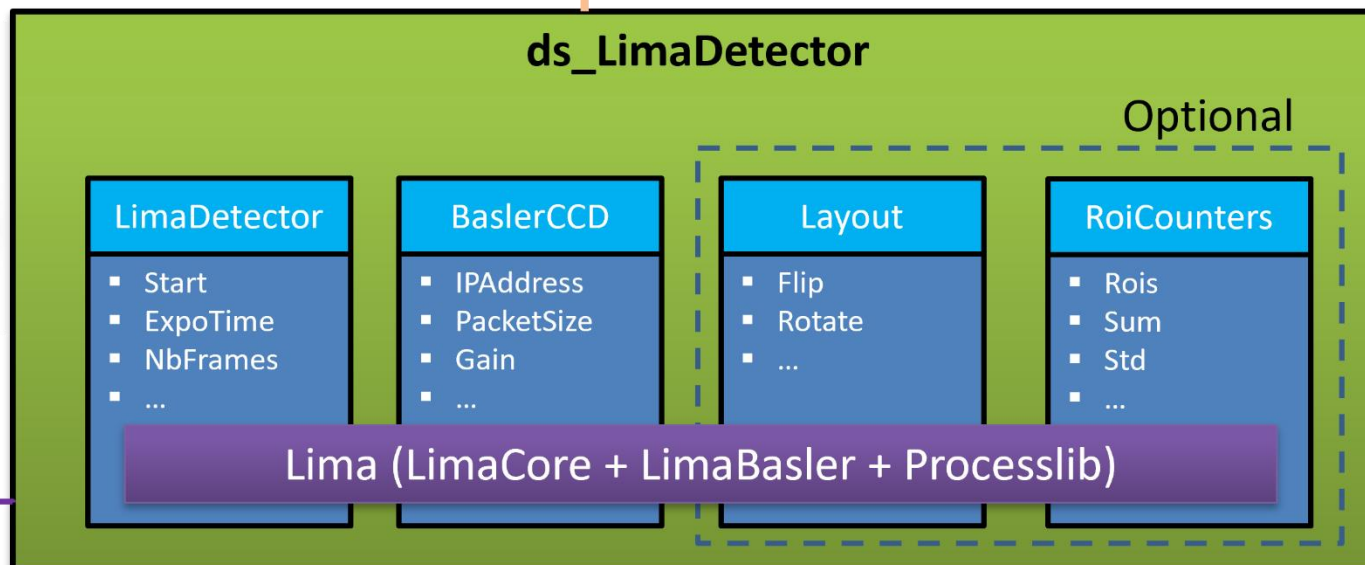


<https://lima1.readthedocs.io/en/latest/>

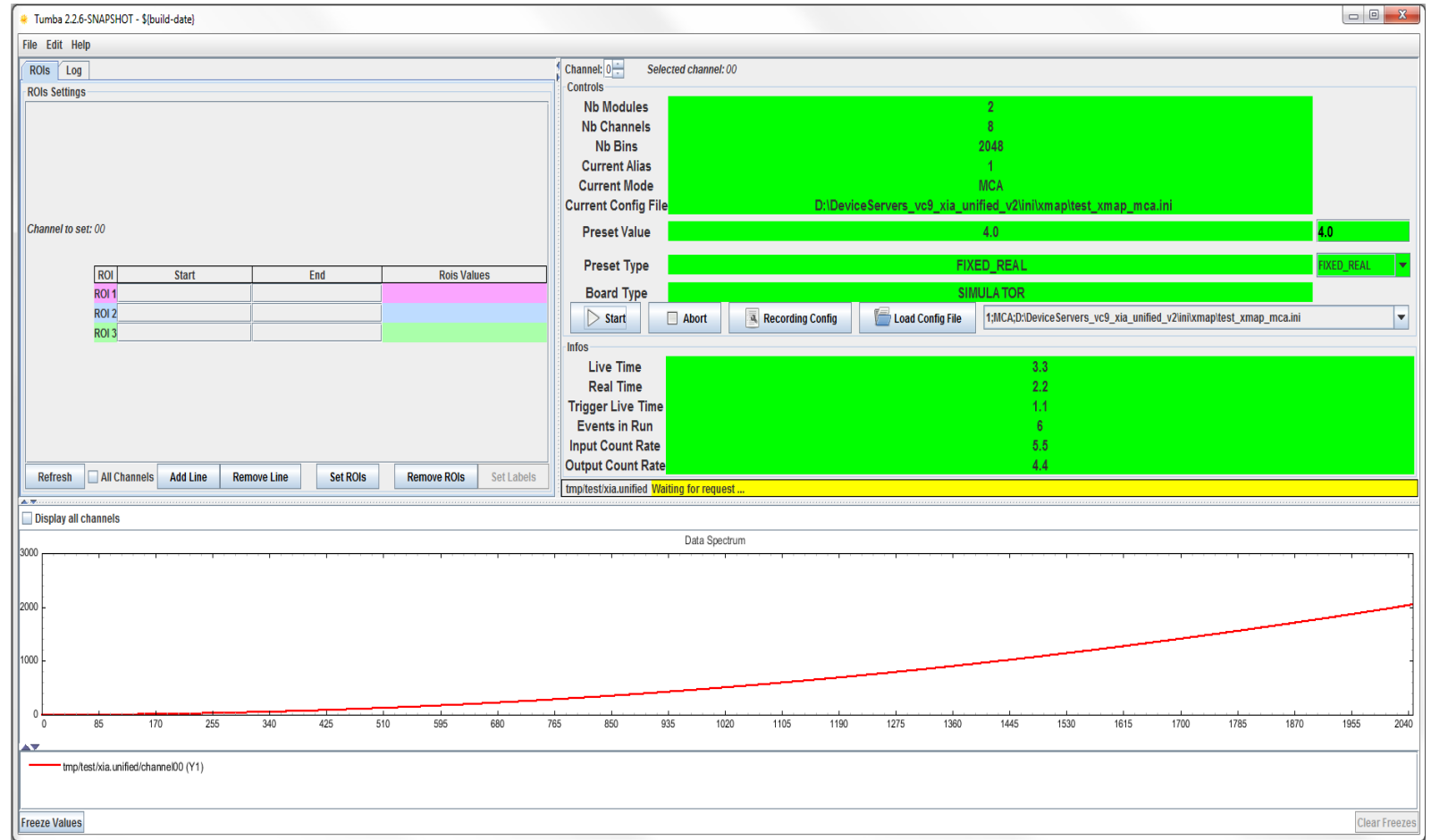
<https://lima-tango-cpp.readthedocs.io/en/master/>



TANGO Software bus

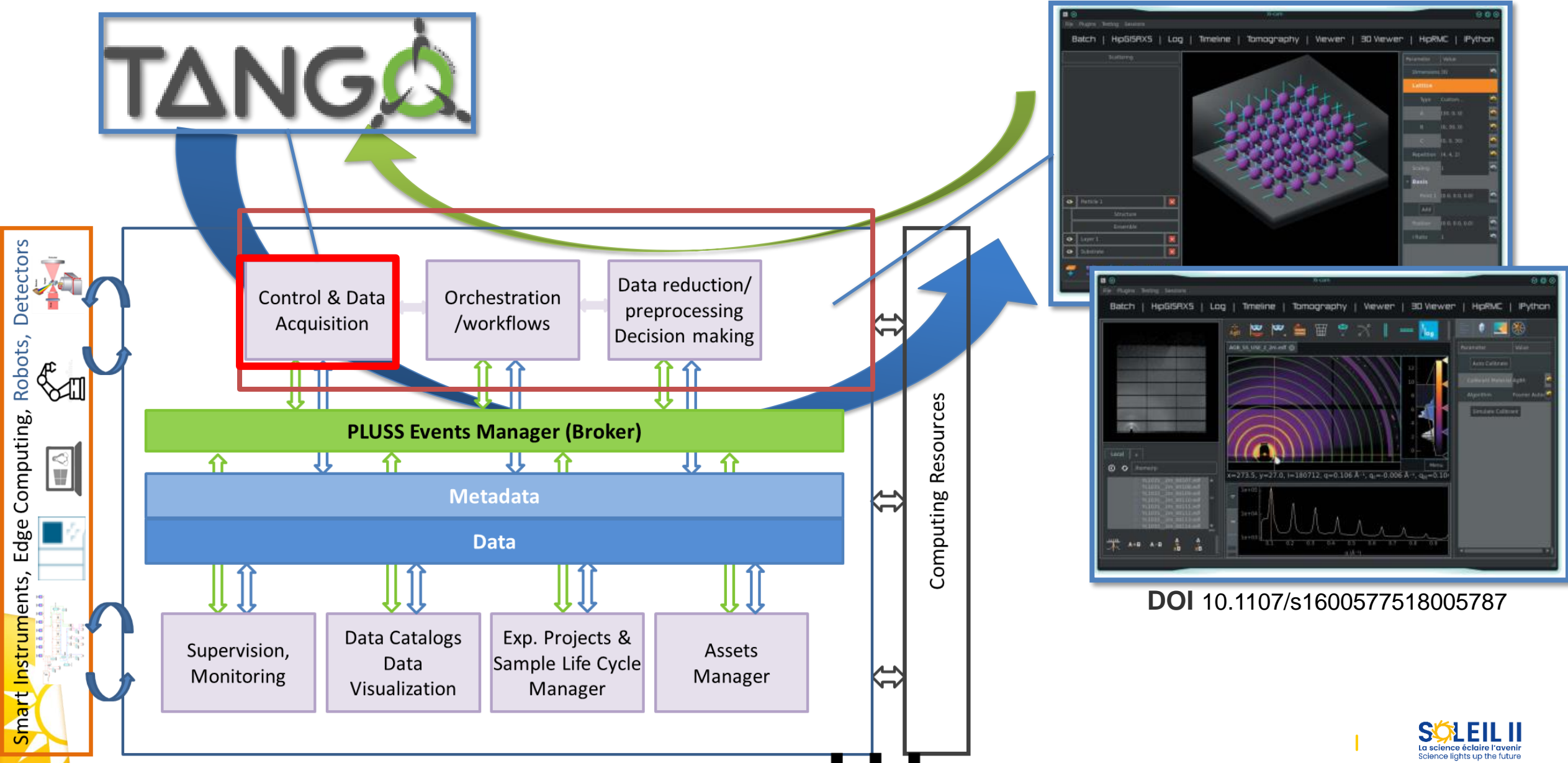


- XIAs
 - Xmap
 - Falcon
- Xspress3
- DanteDpp
- Not a standardized lib as Lima
- But trying to get a standardized Tango interface



Acquisition system perspectives

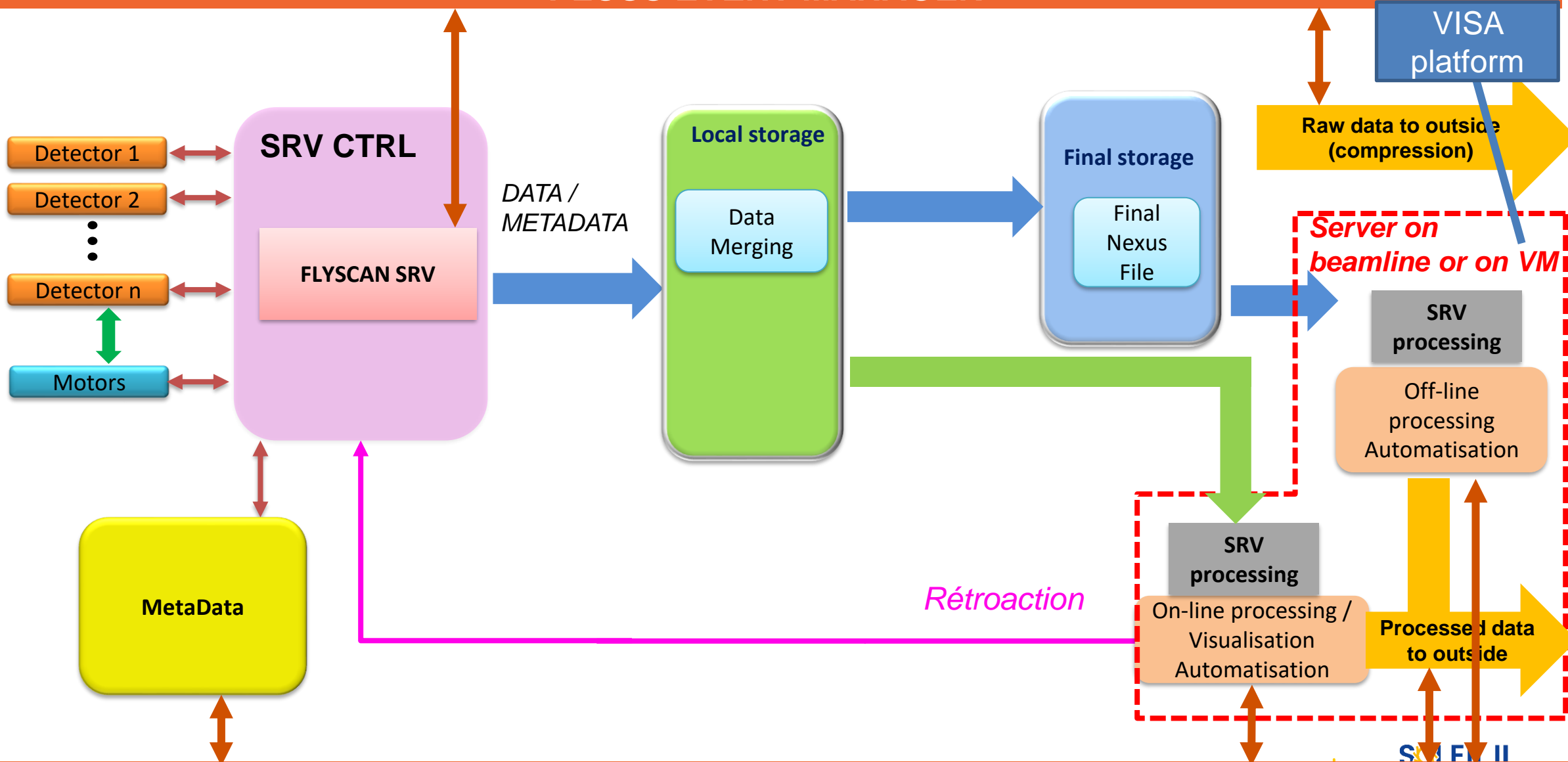




- **Hardware systems**
 - Put MTCA systems on production for SOLEIL
 - HW, FW, SW standardization and development
 - MicroTCA systems monitoring (Zabbix under evaluation)
 - PandABox Gen 2
 - Migrate legacy/obsolete systems to new products
- **Software systems**
 - Decommissioning of the ScanServer: towards Flyscan
 - Flyscan upgrade
 - With automatic retroaction
 - Visualisation improvement
 - Connected to PLUSS* (event & api manager)
 - * see Gwenaelle's DataManagement slides

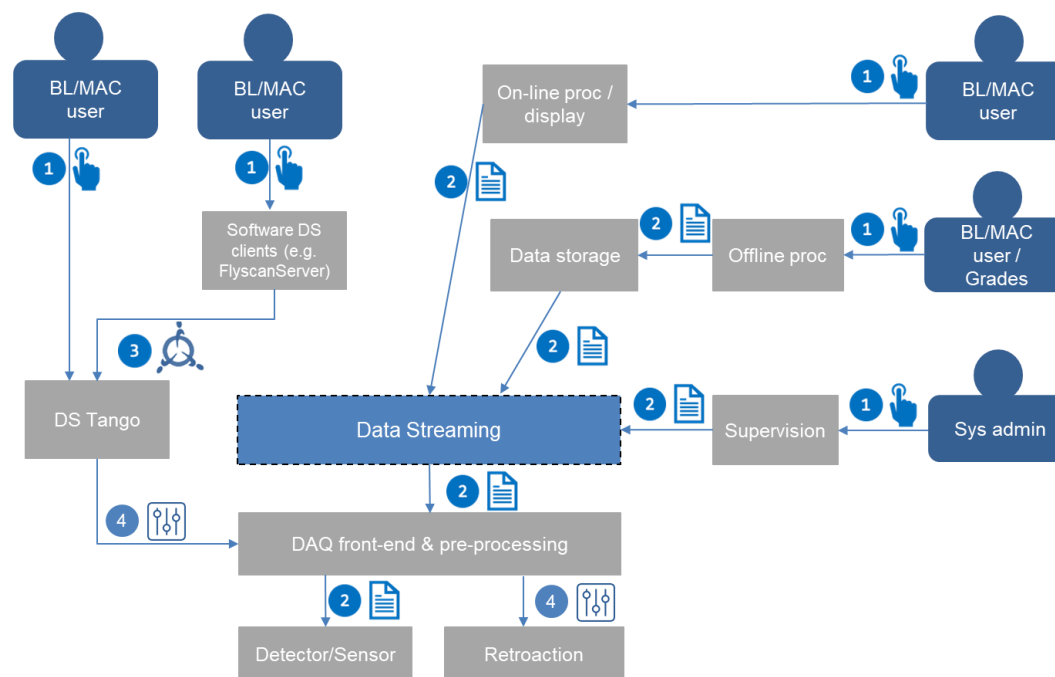
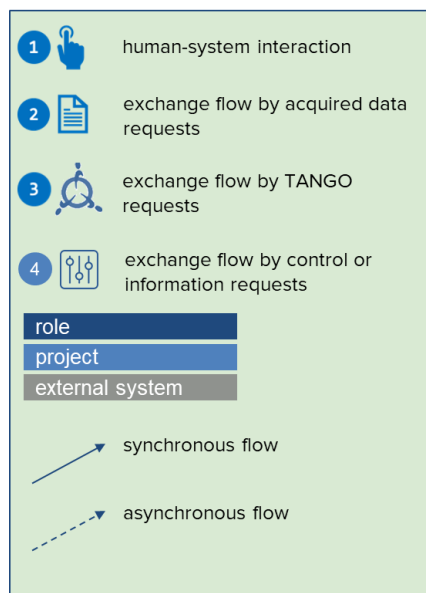


PLUS EVENT MANAGER



- Data Streaming

- New solution for future requirements
- Lima2, ASAPO, Hidra, Odin, DataStaMP ...
- Interaction with PLUS



- Questions
 - MicroTCA generic framework ?
 - MicroTCA monitoring / supervision ?
 - Embedded SW: CI/CD ?
 - Which GUI for detectors ?
 - Data / Metadata streaming ?
 - which ?
 - Lessons learn on selection ?
 - Data reduction at edge computing (GPU, FPGA) ?
 - Post processing automation

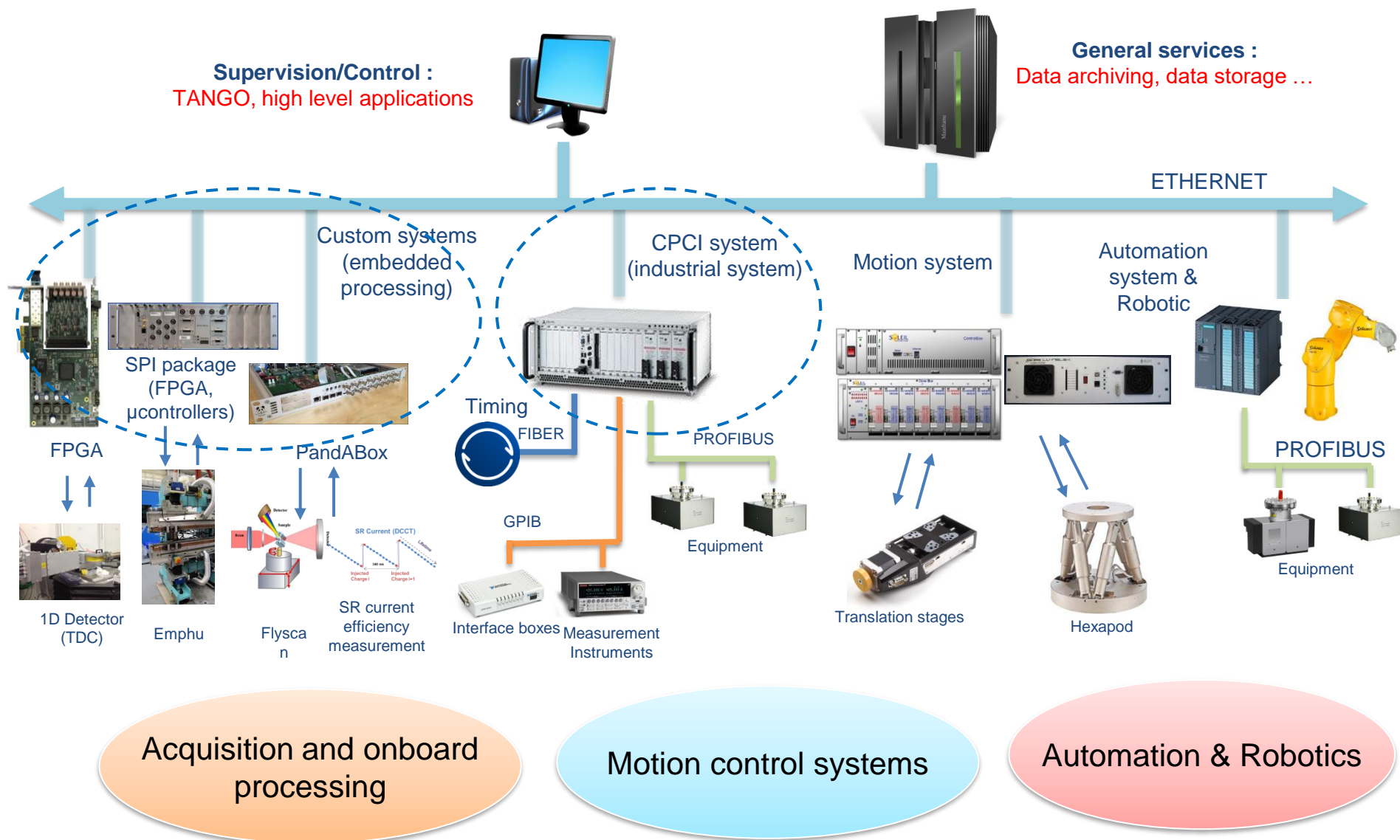


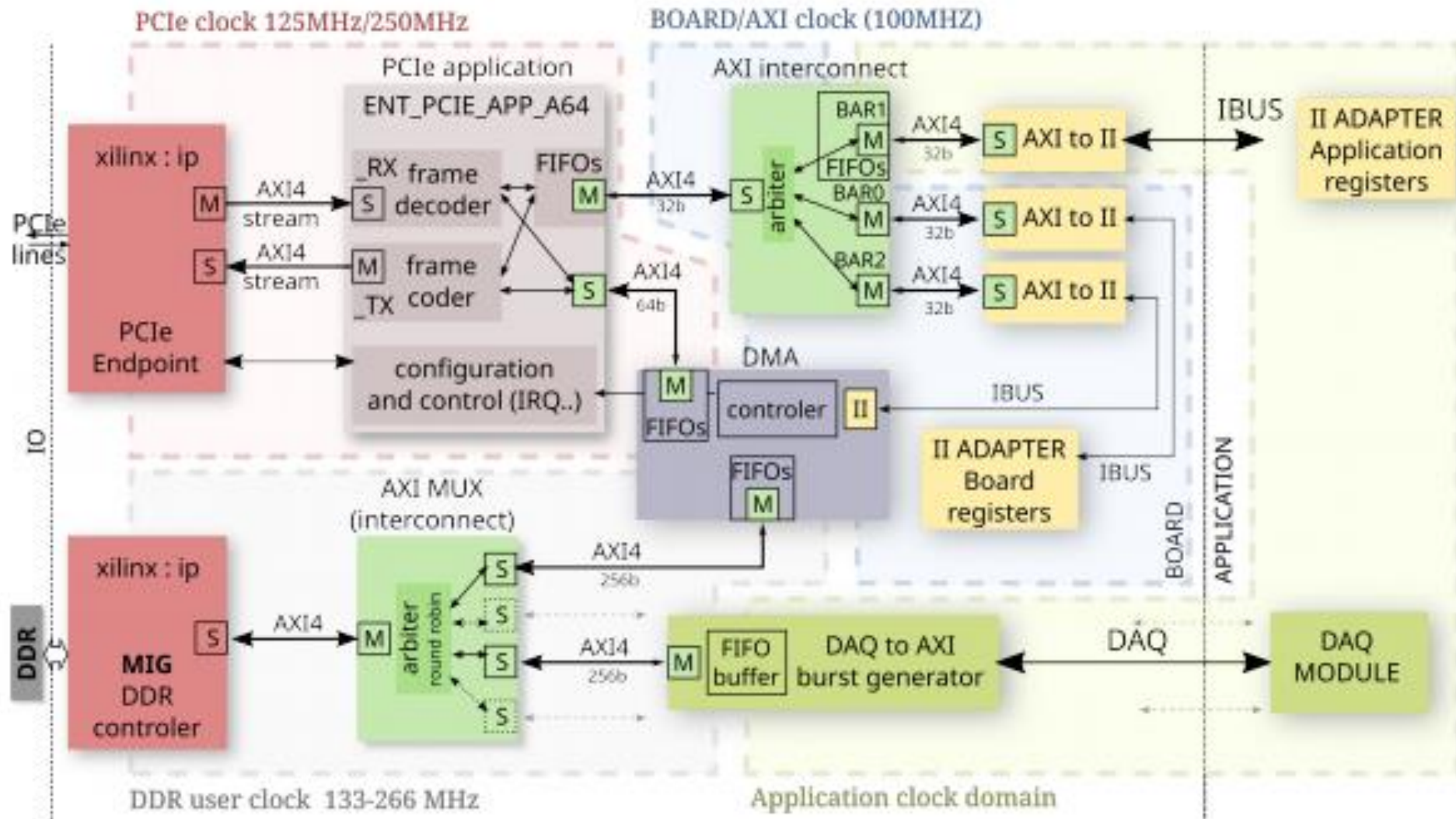
Thank you!



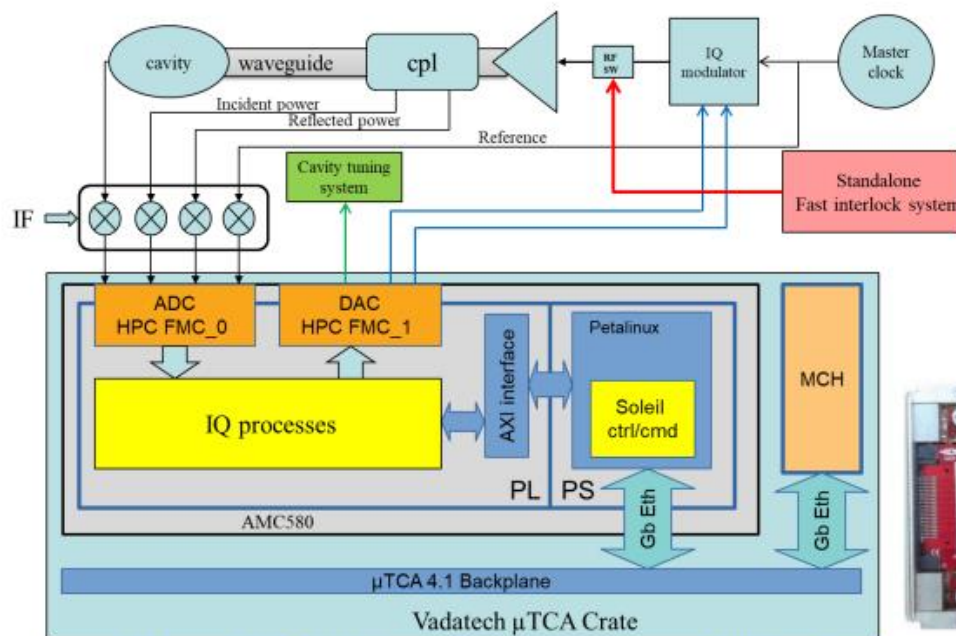
Backup slides



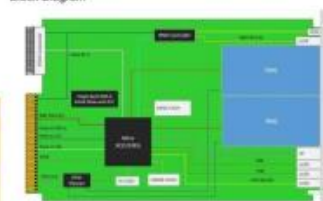




SOLEIL The progress of the DLLRF on MicroTCA



Block Diagram



- 4 channels ADC FMC board (TECHWAY) successfully interfaced into the Zynq of the ZC706 evaluation board, IQ process tested and validated
- Configuration and setup of Vadatech MicroTCA: done
- Migration of the previous development to the AMC580 (Vadatech) board is successful
- Development of python socket server on PS side for communication is done
- Interfacing of DAC FMC board (FMC224) is ongoing
- Interoperability difficulties during development: Vadatech AMC580 seems not working on NAT MicroTCA rack
- After repairing of the power supply of AMC580, we never tried it again and AMC580 is working fine on Vadatech rack

Today status: The main deal is to interface the DAC FMC.
Then all IQ process are ready to be implemented.



PandABox project

(Position and Acquisition)



- Initial objectives

- Connecting **Motion Control** Systems and **Data Acquisition** Systems for simultaneous and multi-technique scanning applications
- Providing Encoder Processing, Common Synchronous Triggering and Data Captures

- Motivations

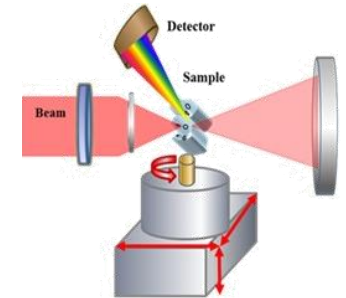
- Managing obsolescence and limitations
- Maintaining modularity
- Improving performance

- Organisation

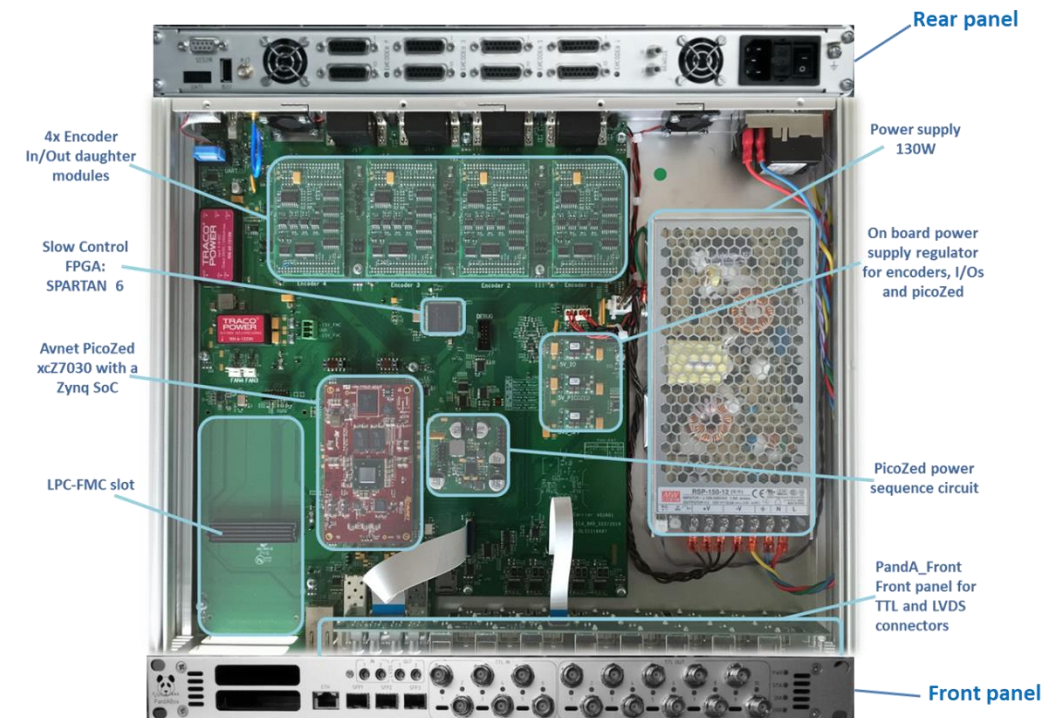
- Development collaboration between SOLEIL and Diamond
- Task sharing
 - SOLEIL: Electronics and Mechanics
 - Diamond: Firmware, Software and Web GUI

- Resulting system

- **Flexible** design solution, **open** and **extensible** platform
 - Modular hardware with removable modules
 - Firmware and software easily configurable and adaptable

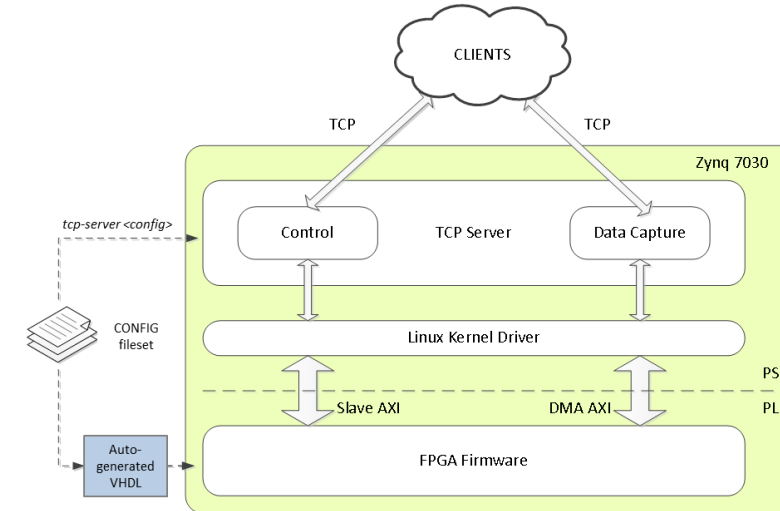
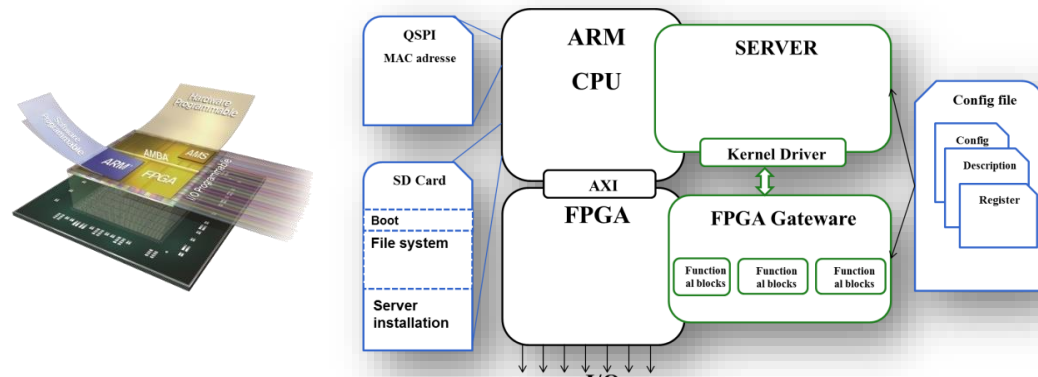


- Packaged in a 19" 1U rack
- Platform developed around an off-the-shelf product:
 - Avnet PicoZed Z7030 module based on a Xilinx Zynq 7030 SoC (System On Chip)
- HW architecture around PicoZed and I/O interfaces
 - 4-Channel Encoders I/Os (Quadrature, SSI, BiSS-C, EnDat)
 - TTL and LVDS I/Os
 - 1 Gigabit Ethernet for Control and DAQ
 - 3 SFP ports
 - FMC LPC slot
 - On board clock tree & power supplies
 - Slow control via a Xilinx SPARTAN-6 FPGA:
 - Temperature monitoring
 - On-board power supplies voltage monitoring
 - Fan-speed monitoring
 - Configurations of the I/O encoder signals
 - Front panel configurations
 - JTAG for SoC and FPGA debugging
 - RS-232 serial console terminal
 - USB host for firmware upgrades

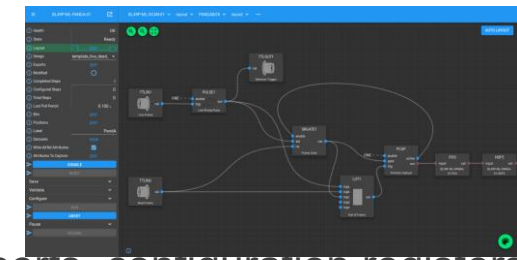


https://www.ohwr.org/project/pandabox-hw/blob/master/PandABox_User_Guide.pdf

- Flexible and configurable architecture



16th Int. Conf. on Accelerator and Large Experimental Control Systems
 ICALEPCS2017, Barcelona, Spain JACoW Publishing
 ISBN: 978-3-95450-193-9 doi:10.18429/JACoW-ICALEPCS2017-THPHA068



- **FPGA firmware layer (PL)**

- Structured into numerous Functional Blocks (FBs)

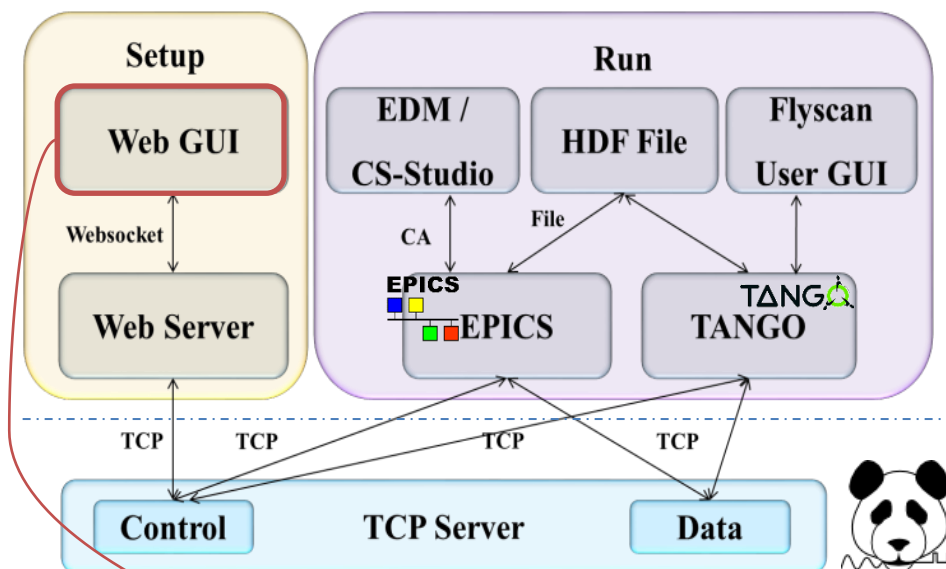
- **TCP-Server layer (PS)**

- **Two socket endpoints** to connect to clients (EPICS, TANGO, etc.)
 - configuration **control** (control & status register)
 - streamed data **capture** (interface with DMA engines for synchronous R/W)

⇒ 2 layers **tightly coupled** through a **common set of configuration files** (FB's I/O ports, configuration registers, and descriptions)

⇒ Allowing to **design and compile** a custom set of **FBs** into the **firmware** with **access from the TCP Server**

- Fully **re-wirable** (at run-time) architecture



• TCP Server

- To interface with either **TANGO** Device Server, **EPICS** IOC, or web-server

• Web GUI

- Visualizing and wiring the functional blocks
- Setting the functional blocks' parameters
- Help to build customized applications

